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10/625,285	07/22/2003	Peter R. Munguia	P16384	7500

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,285	MUNGUIA ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-33 and 35-48* is/are rejected.

7)☒ Claim(s) *34 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set for in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.1 14. Applicant's submission filed on 8/14/06 has been entered.

Claims 1-23 have been presented for examination in this application. In response to the last office action, claims 1-23 have been canceled, claims 24-49 have been added. As the result, claims 24-49 are now pending in this application.

On 10/12/2006, a telephonic interview was conducted with Applicant's representative Jose M. Matta #56978, Examiner requests clarifications for the meaning of independent claim 24 in regard to a controller and the distinguishing among boot, reset or other pre-configuration state of the apparatus. Examiner also suggests using the phrase "generating an unencode.." in lines 25,26 and removing the "to generate" in line 2 of the claim 24. Examiner request Applicant reviewing other claims for similar defect.

Subsequently, Applicant faxed to Examiner on 10/20/06 potential amendments to claims.

On 10/23/06, a telephonic interview was conducted with Examiner, Examiner's supervisor Huyng S. Sough, Applicant's representatives Jose M. Matta #56978, Vince Anderson #54962 regarding the potential amendments to claims. Examiner's supervisor suggests in claim 24, amending line 2 to indicate "controller configured to generate", and similar amending to other claims if necessary, Examiner also requests for the clarification between boot and reset in claim 24.

On 10/24/06, Applicant faxed to Examiner a correspondence to indicate that Applicant will not be filling the potential amendments in this matter.

Therefore, this Office Action is replied to the amendments/remarks filed on 8/14/06.

Applicant's amendments/remarks filed 8/14/06 have been fully considered with the result as follows,

Applicant's amended specification's page 8, table 1 overcomes the drawing objection in previous office action.

Claims 24,38,41,48 are rejected.

Claims 34,49 are objected to.

Claim Objections

Following claims are objected to because of the following informalities:

As in claim 24, "the same boot device" lacks antecedent basis.

As in claims 29,32,33, "the selected boot device" lacks antecedent basis.

As in claims 35,37, "the boot device(s)" lacks antecedent basis.

Appropriate correction is required.

U.S.C. 112, first paragraph

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 24,38,41,48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, has possession of the claimed invention.

As in claim 24, the claim recites "..controller initialization during boot, reset, or other pre-configuration state of the apparatus".

Examiner cannot find support in the specification that distinguish boot, reset. Further more, Examiner cannot find any embodiment in the specification that supports the pre-configuration state of the apparatus.

Specification's paragraph 23 line 3 merely recites the above claim's limitation. It states "system power-up, a system reset, or some other event".

It is not clear the differences of boot (system power up) and reset (system reset), because it's commonly known in the art that reset (system reset) includes system power up. In the telephonic interview on 10/12/06, Applicant's representative indicates the reset somehow direct to the "warm boot". If that is the intent of the Applicant, Examiner requests further expressly clarification the claim, because it's not commonly known in the art that reset represents "warm boot".

Examiner also request clarification regarding the phrase "other configuration state of the apparatus", since it is not clear what "other configuration state of the apparatus" is.

Claims 38,41,47 have the same defect as of claim 24.

All dependent claim(s) are rejected as having the same deficiencies as the claims they depend from.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-33,35-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over William et al (US 6199151).

As in claim 24, the claim recites an apparatus comprising: a controller, to generate, before controller initialization during boot, reset, or other pre-configuration state of the apparatus,

an unencoded chip select word in response to a default unencoded chip select mode,

an encoded chip select word in response to a default encoded chip select mode; and

wherein the encoded chip select word and the unencoded chip select word select the same boot device.

William discloses a method and apparatus to provide chip selects in either encoded or unencoded words to address any memory devices. William discloses a computer system (corresponding to the claim's apparatus) comprising a controller (William's Fig 1: #12 subsystem controller). William's controller further comprises address translation elements. (William's Fig 4, TLB table, address decode logic, chip select logic) that capable of providing the address lines and chip select lines to address any memory devices. The chip select word can be either an unencoded chip select word (William's Fig 3, CS: bits 8-1), or encoded chip select word (William's Fig 3: CS bits 2-0). Both unencoded chip select word and encoded chip select word select the same memory device, for example, in Fig 3, values "00000010" and "001" points to the same memory device (William's column 6, lines 33-50). William clearly teaches the need to quickly provide addresses, and chip select signals to memory devices and thereby improve the performance of the overall system. In this instance, William teaches a novel approach that is the controller itself with its associating logic can quickly handle chip select values in both encoded and unencode forms and quickly provide individual chip select lines to memory devices (Williamn's column 1 lines 37-46, column 2 lines 6-15). Although William does not expressly discloses that the memory device stores the code to initializing the system. However, it's well known in the art that memory devices are used to stored variety of codes including boot code, initializing code, operating system code, application code. Thus William's controller is clearly intent to provide quick chip select lines to any memory devices in any period of time and thereby further improve the performance of the overall system.

As in claim 25, the claim recites wherein the controller comprises a memory controller

to generate the encoded chip select word and the unencoded chip select word. The claim rejected based on the same rationale as of claim 24. William's Fig 1: #12 discloses subsystem controller corresponds to the claim's memory controller to generate the encoded chip select word and the unencoded chip select word (William's column 6 lines 13-26).

As in claim 26, the claim recites wherein the memory controller comprises an address decoder to generate the encoded chip select word and the unencoded chip select word (William's column 6 lines 18-25, logic to generate encoded row values to be stored in TLB).

As in claim 27, the claim recites wherein controller initialization comprises configuration of the controller to operate in an encoded chip select mode or in an unencoded chip select mode (William's column 6 lines 1-6 discloses the controller capable of being configured to operated in encoded chip select mode and/or in unencoded chip select mode).

As in claim 28, the claim recites wherein the controller comprises a configuration store to store configuration data to configure the controller to operate in an encoded chip select mode or in an unencoded chip select mode. The claim rejected based on the same rationale as of claim 27. William's column 6 lines 1-6 teaches the controller capable being configured to operated in encoded chip select mode and/or in unencoded chip select mode, therefore inherently the configuration information must be stored in some storage elements in order to convey to the controller the modes in which the controller must be operated on.

As in claim 29, the claim recites wherein the selected boot device comprises a memory device. It's a well known in the art that a memory device is used to boot the system.

As in claim 30, the claim recites wherein the unencoded chip select word comprises a first bit pattern and the encoded chip select word comprises a second bit pattern and the first bit

pattern includes the second bit pattern William's Fig 4 discloses the unencoded chip select word/first bit pattern includes the encoded chip select word/second bit pattern. For example in Fig 4 row 2, the CS 8-1 bit pattern "00000010" includes the CS 2-0 bit pattern "001".

As in claim 31, the claim recites wherein the lowest order bits of the first bit pattern include the second bit pattern. William does not expressly disclose the claim's limitation. However William clearly suggests the controller capable and intent to provide with any encoded bit pattern, any sequential binary values (see William's column 6 lines 2-6).

As in claim 32, the claim recites wherein the controller to generate the encoded chip select word and the unencoded chip select word in response to an address for a boot code nub and the selected boot device comprises the boot code nub. The claim rejected based on the same rationale as of claim 24. William's column 5 lines 35-60 discloses the controller having configuration registers to store addresses of different memory devices being used during different period of time, therefore, it is understood that these configuration registers including addresses of memory devices for storing any data including application code, operation system code, boot code etc.. Furthermore, these configuration registers can be easily programmed with pre-determined values at start up time whether by BIOS code (as an example disclosed in William's column 5 lines 40-47) or some well known techniques in the art, for example pre-setting registers values by using tie up/down resistors, read only registers or by scanning in pre-determine values at start up time.

As in claim 33, the claim recites wherein the controller, to generate the unencoded chip select word for the address such that the unencoded chip select word comprises exactly one

active chip select bit that corresponds to a predetermined chip-select line used to select the boot device; and the controller to generate the encoded chip select word for the address such that the encoded chip select word comprises exactly one active chip select bit that corresponds to the predetermined chip-select line. The claim rejected based on the same rationale as of claim 32. William's column 6 lines 40-50 disclose an individual physical chip select line CS1 to CS8 is corresponding to the encoded chip select and the unencoded chip select. William's Fig 4 row 2 further discloses one active bit of the unecoded chip select corresponds to one active bit of the encoded chip select.

As in claim 35, the claim recites wherein the encoded chip select word is generated according to an encoding scheme to assign numbers to the boot devices, the numbers to range from one to a number greater than one. The claim rejected based on the same rationale as of claim 32. William's column 5 lines 35- discloses of using configuration registers that can map address of any code stored to any memory device, wherein the number of devices to store code can be more that one (William's Fig 1; 15).

As in claim 36, the claim recites wherein the encoded chip select word is to encode the number one (see William's Fig 3 row 1, encoding the number one "00000001").

As in claim 37, the claim recites wherein the controller, in response to an address for a boot code nub that does not map to the boot device, converts the address to an address that does map to the boot device. The claim rejected based on the same rationale as of claim 32. William's column 5 lines 35-56 further discloses by matching address with the configuration registers, one can easily determine the address corresponding to a particular device. For example, if the address does not match address range in a first device, the address is further compared and if it matches

address range of the second device, the address is converted to the physical address and chip select of the second device.

Claim 38 rejected based on the same rationale as of claim 24. William's column 6 lines 1-6 further disclose the chip select word can be figured and used with any encoding schemes.

As in claim 39, the claim recites wherein the device storing the boot code nub is coupled to the apparatus via a predetermined chip select line, each of the other devices of the plurality of devices is coupled to the apparatus via a separate chip select line; and wherein the apparatus activates the predetermined chip select line coupled to the device storing the boot code nub, regardless of whether the chip select word is encoded or unencoded. William's Fig 2, column 6 lines 35-50 discloses the memory device (Fig 2: #16A) is coupled to a predetermined chip select lines CS1, and the memory device (Fig 2: #17A) is coupled to a predetermined chip select lines CS2. Furthermore, it's well known in the art that the memory devices are used to store any codes (operating system, BIOS, boot code, application code). William's Fig 3 row 2 discloses both unencoded chip select and encoded chip select points to the same physical chip select line.

As in claim 40, the claim recites comprising a chip select decoder coupled to the apparatus and coupled to each of the devices of the plurality of devices via a separate chip select line, wherein, the chip decoder activates the chip select line of the device with the boot code nub in response to receiving the chip select word, regardless of whether the chip select word is encoded or unencoded. The claim rejected based on the same rationale as of claim 39. Furthermore, in order to generate the physical chip select from encoded chip select and

unencoded chip select as showed in William's Fig 3, inherently a chip select decoding logic must be employed.

As in claim 41, the claim recites generating on an apparatus, in response to an address for the boot code nub and during boot, reset, or other pre-configuration state of the apparatus, a chip select word that, if the apparatus is in a default unencoded chip select mode, results in selection of a boot device storing the boot code nub, and if the apparatus is in a default encoded chip select mode, results in selection of a boot device storing the boot code nub.
William discloses a method and apparatus to provide chip selects in either encoded or unencoded words to address any memory devices. William discloses a computer system (corresponding to the claim's apparatus) comprising a controller (William's Fig 1: #12 subsystem controller). William's controller further comprises address translation elements (William's Fig 4, TLB table, address decode logic, chip select logic) that capable of providing the address lines and chip select lines to address any memory devices. According to William's method, the chip select word can be either an unencoded chip selects word (William's Fig 3, CS: bits 8-1), or encoded chip select word (William's Fig 3: CS bits 2-0). Both unencoded chip select word and encoded chip select word select the same memory device, for example, in Fig 3, values "00000010" and "001" points to the same memory device (William's column 6, lines 33-50). William clearly teaches the need to quickly provide addresses, and chip select signals to memory devices and thereby improve the performance of the overall system. In this instance, William teaches a novel approach that is the controller itself with its associating logic can quickly handle chip select values in both encoded and unencode forms and quickly provide individual chip select lines to memory devices (William's column 1 lines 37-46, column 2 lines 6-15). Although William does not expressly

discloses that the memory device stores the code to initializing the system. However, it's well known in the art that memory devices are used to stored variety of codes including boot code, initializing code, operating system code, application code. Thus William's controller clearly suggest to provide quick chip select lines to any memory devices in any period of time and thereby further improve the performance of the overall system.

As in claim 42, the claim recites executing the boot code nub, and in response to executing the boot code nub, updating one of the default unencoded chip select mode and the default encoded chip select mode to one of an unencoded chip select mode and an encoded chip select mode. Examiner notes that the claim can be understood as followings, in response to executing the boot code nub, the mode of the chip select is not changed. The claim rejected based on the same rationale as of claim 41. William's column 6 lines 1-5 further disclose the controller can be configured to operate in any encoding schemes.

Claim 43 rejected based on the same rationale of claim 33.

Claim 44 rejected based on the same rationale of claim 31.

Claim 45 rejected based on the same rationale of claim 35.

Claim 46 rejected based on the same rationale of claim 36.

Claim 47 rejected based on the same rationale of claim 38.

Claim 48 rejected based on the same rationale of claim 35.

Allowable Subject Matter

Claims 34,49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

As to the remarks on pages 9-11,

regarding, the objections to the specification, the amended specification overcomes the objection in previous office action;

regarding allowable subject matter, claim rejections under 35 U.S.C 101 and premature finality of office action. These issues are mooted, since new set of claims 24-49 are added.

As to the remarks on pages 11-14 regarding the rejections under 25 U.S.C 102, these issues are mooted, since new set of claims 24-49 are added.

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private.PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER